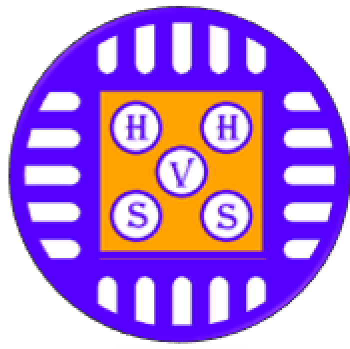


HVSTECH LLC

SIMPLIFYING NETWORKING SOLUTIONS FURTHER

COMPANY PROFILE

2622 MEADOW GLEN DR.

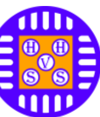
SAN RAMON, CA 94583

PHONE : 1-408-406-1118

EMAIL : info@hvstechllc.com

SUMMARY

- About Us
- Why HVSTECH?
- Organization Structure
- Our Capabilities & Services
  - Hardware Design
  - PCB Layout Design
  - IC Package Design
  - PCB / IC Design Simulations
  - PCB Manufacturing & Assembly
- Appendix



ABOUT US

- HVS offers One-Stop Solution for System / Board Design / High Speed IC Package and PCB Design Services right from the Schematic to Layout to simulation to Manufacturing & Assembly.
- Serving International Semiconductor Industry for more than 12 years.
- Strong 25 Member Team in India office and efficient 2 Member Team in USA office.
- More than 30 years of combined Semiconductor Industry experience
- Office Locations shown below.

USA OFFICE
==========
2622 Meadow Glen Dr.
SAN RAMON, CA – 94583
USA
CELL : 1 408 406 1118
EMAIL: info@hvstechllc.com

INDIA OFFICE
============
TBD

WHY HVS?

- Understand the Importance of Customer Service & Satisfaction :
  - Provide quote within 24 Hours, Very quick and flexible with ECO & other paperwork.
  - Respond to any other paperwork activities within 24 hours.
  - No After-Hour meetings with overseas team. All meetings done during US office Hours.
- Understand the Importance of Real-Estate :
  - Planning start from lowest layer count and smallest form factor, at the same time, keep quality and reliability as ultimate goal.
- Understand the Importance of Deadlines :
  - Deadline is defined first and all milestones scheduled around it.
  - Round the clock shifts available, for fast turn around time.
  - Pay Attention to details, use Result Oriented approach.
- Understand the Importance of Time-To-Market
  - Working under time-crunch and in crisis situation is our Specialty. Handled multiple such projects successfully with ease.
  - Can visit customer site in USA in person, if required.

CAPABILITIES & SERVICES

IC Package Design

PCB Manufacturing & Assembly

Pre & Post Layout Sims

PCB Layout Design

Hard-ware Design

Turnkey Service

DESIGN SUPPORT STRUCTURE

Design Services

System / Board Design

- Customer Collateral
- Architecture Development
- Schematics Design
- Pre/Post Layout SI & PI
- Netlist & BOM Generation

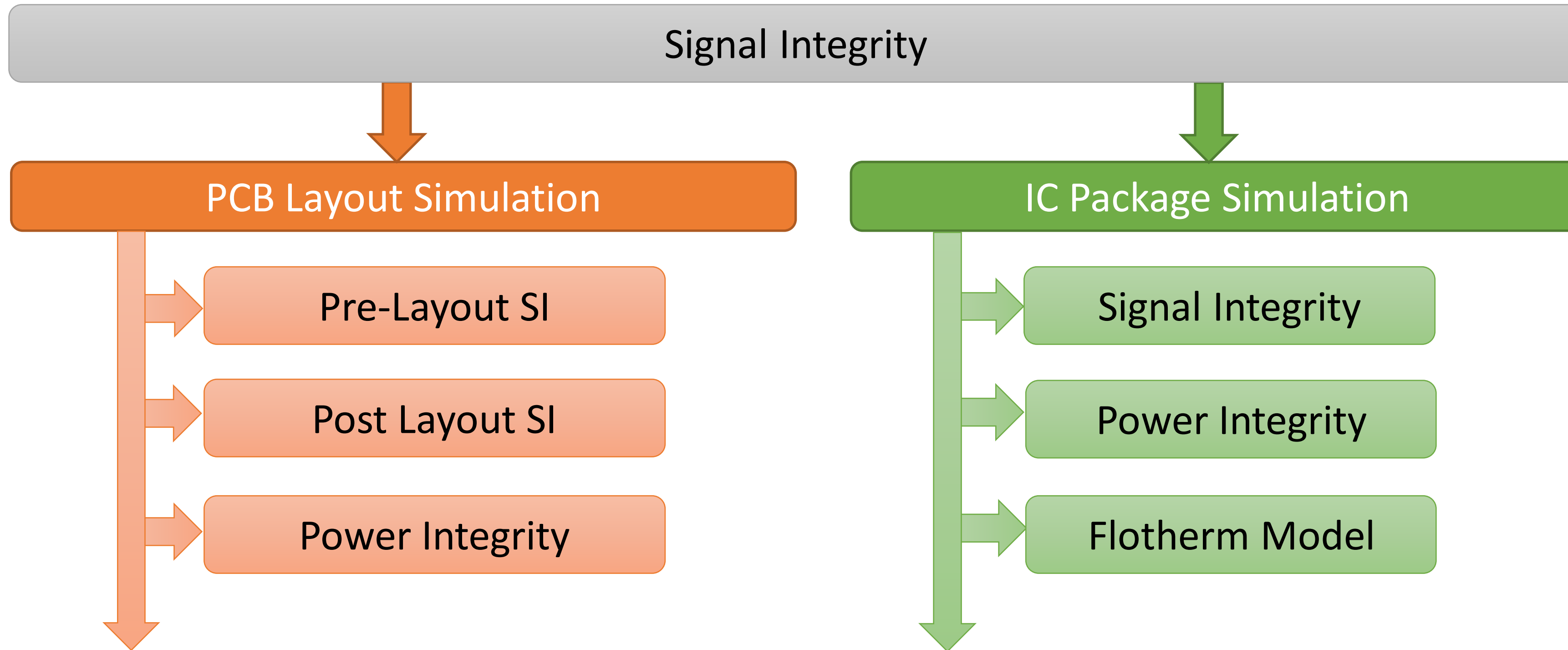
PCB Layout Design

- Footprint Creation
- Netlist Import
- Placement Floorplan
- Stackup Defn & Constraint Mgmt.
- SI & PI
- Gerber Validation
- Fab & Assy Support

IC Package Design

- Package Feasibility Study
- SI & PI
- BGA BallMap Defn
- PCB Feasibility Study
- Reference Designs
- Design Guidelines

SIMULATION SUPPORT STRUCTURE



PCB MANUFACTURING SUPPORT STRUCTURE

PCB Manufacturing

- PCB Fabrication
- PCB Assembly (Consigned / Turnkey)
- PCB Bringup / Testing

DOMAIN EXPERTISE

Design Features

Hardware Design

- Chip Level Product Design
- Board Level Product Design
- Reduced Footprint Product Design

PCB Layout Design

- High Speed/HDI Design
- Analog & Power Supply Designs
- Probe Cards & ATE Loadboards
- HTOL / Burn-In Boards
- BHAST Boards
- Dye-N-Pry Boards
- BLR Boards

IC Package Design

- FCCSP
- FCBGA
- FCLGA
- WireBond

SYSTEM DESIGN : HARDWARE DESIGN FEATURES

Our Hardware Design Services can be broadly classified in 3 categories:

- **Chip Level Product Design**: We can help you design all the Hardware required to take your silicon to production. This involves designing, Substrate (IC Package), Test Boards (SLT/BLT/ATE loadboards / Wafer Probe Cards), Quality and Reliability Boards (Burn-in Boards / BHAST Boards / Dye-N-Pry Boards)

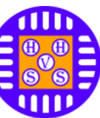
- **System Level Product Design**: we can help take your concept to the final product. Examples of system Level Product would be NIC Card or SFP Module.

- **Reduced Footprint Product Design**: We consider ourselves specialist in combining multiple technologies together to create a product with reduced footprint. This not only simplifies the System Level Design from end customer point of view, but helps achieve faster time to market for the main product.

PCB TOOLS

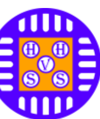
- PCB SCHEMATICS
  - OrCAD Capture
  - Concept HDL
  - Altium
  - Powerlogic

- PCB LAYOUT
  - Cadence Allegro
  - OrCAD Layout Plus
  - Altium
  - PowerPCB



PCB DESIGN SUMMARY

- Extensive experience with Layout design for High Speed (56G) & Mixed Signal / High Layer Count / Large Form Factor System Level PCBs as well as Test & Reliability Boards.
- Provide additional supporting design services, like Schematic Design including BOM generation and Enclosure Design with thermal considerations.
- Expertise in Signal Integrity and Power Integrity Analysis for the PCB designs. Can also provide Pre-Layout simulation, if required.
- We partner with some of the top domestic and offshore PCB manufacturers and Assembly Houses, to offer the highest quality PCBs at the most competitive prices.
- Overall, we provide Full Turnkey Design support for your project; (Sch + Layout + Enclosure + PCB Build)

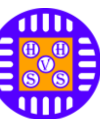


PCB FEATURES SUMMARY

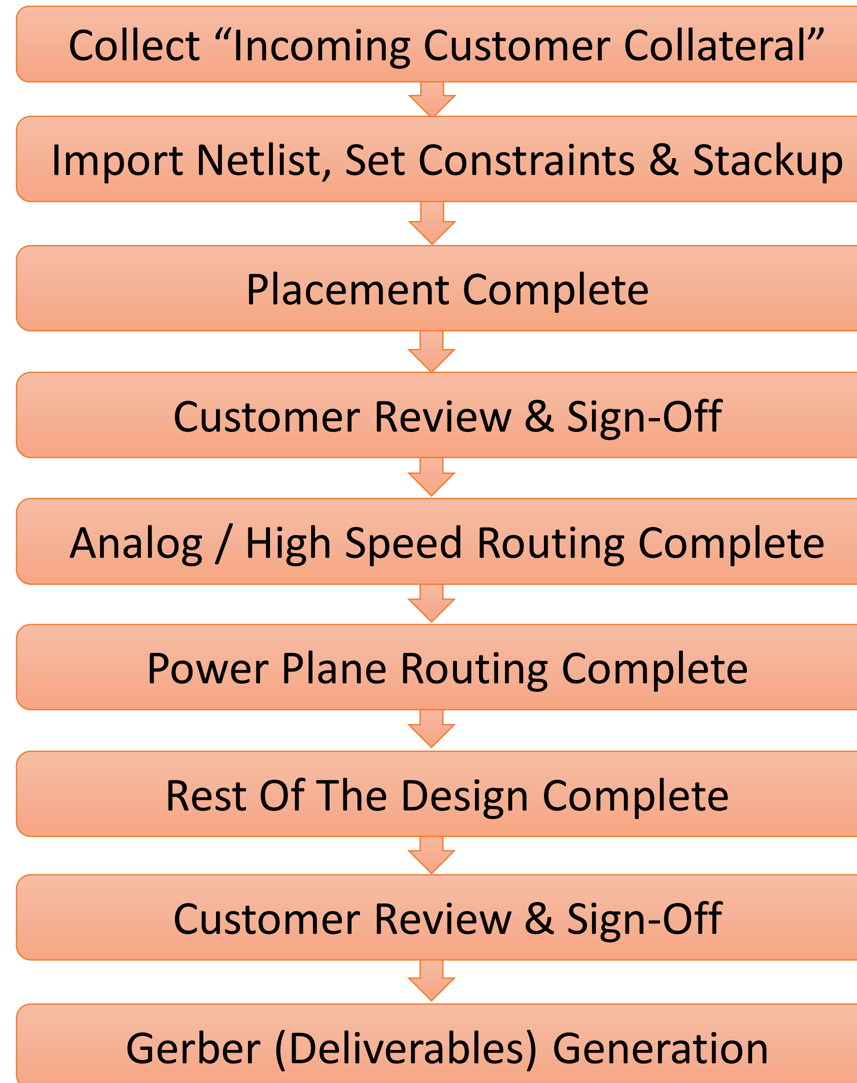
PACKAGE FEATURES	DESCRIPTION
Max Speed	Upto 56G (NRZ)
Layer Count	4 to 30
Minimum Trace Width/Space	3mils / 4mils
Via Type	Through / Blind / Buried
Via Drill Size	5/5
Via Pad Size	3mils to 24mils
Diff Pair Coupling	Edge Coupled / Broad Coupled
Interfaces	PCIE Gen-2/3/4/5, XFI, XGMII, XAUI, USB2/3, QDR, SATA,GRMII, FSB, IDE,DDR2/3/4
Form Factors	ATX, PCI, PCI-EX, CPCI, PMC, ATCA, AMC NIC, SFP

INCOMING CUSTOMER COLLATERAL

- Project Timeline & Deliverables
- Schematics and PCB Net list
- Stack-up Details
- Mechanical Details / Specs
- Layout Guideline
- Footprints OR Data sheets
- Placement Floorplan
- Other specific requirements

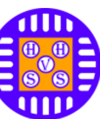


PCB DESIGN FLOW



QUALITY CONTROL

- We are committed to Quality Deliverables.
  - INCOMING COLLATERAL CHECKLIST
  - PHASE-WISE CHECKLIST
  - GOOD TRACKING MECHANISM
  - EFFICIENT PROCESS FLOW APPROACH
  - TWO LEVEL REVIEW



PCB DELIVERABLES

FAB FILES

- Electrical Layers
- Solder Mask Layers
- Silkscreen Layers
- Fabrication Drawing

ASSEMBLY FILES

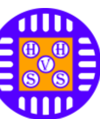
- Assembly Drawing
- Paste Mask Layers
- Placement File (X,Y Coordinates)
- ODB++

Item	Example
Layer Art Files	Projectname_top.art
Paste Mask and Solder Mask files	Projectname_PMT.art
	Projectname_SMT.art
Silk Screen Files	Projectname_TSILK.art
Via Fill Layer	Projectname_viafill.art
FAB	Projectname_FAB.art
IPC-356 Netlist	Projectname_IPC_NET.ipc
NCDrill Files	Projectname_NC_DRILL.drl
Suppor files	art_aper.txt
	art_param.txt
	nc_param.txt

Item	Example
Layer Art Files	Projectname_top.art
IPC-356 Netlist	Projectname_IPC_NET.ipc
NCDrill Files	Projectname_NC_DRILL.drl
Paste Mask and Solder Mask files	Projectname_PMT.art
	Projectname_SMT.art
Silk Screen Files	Projectname_TSILK.art
	Projectname_TSILK.pdf
Assembly	Projectname_TASM.art
	Projectname_TASM.pdf
FAB	Projectname_FAB.art
	Projectname_FAB.pdf
Valor	Brd.txt
	Pad.txt
	Rte.txt
	Sym.txt
XY details	Projectname_xy_body_ctr.txt
	Projectname_xy_pin_1.txt
	Projectname_xy_sym_org.txt
Supporting files	art_aper.txt
	art_param.txt
	nc_param.txt
	nc_tools_auto.txt

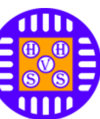
IC PACKAGE : DESIGN/CAD TOOLS

- SCHEMATICS
  - Orcad Capture
- LAYOUT
  - Allegro Package Designer



PACKAGE DESIGN SUMMARY

- More than 25 FCCSP/FCBGA Designs completed
- Can Handle Multiple Designs running in parallel at multiple remote locations.
- Simulation Service (SI and PI) available
- Define BGA ballmap
- Perform BGA Feasibility study in terms of
    - BGA Fanout
    - Decoupling capacitor Placement on PCB
    - High Speed Interface/Bus Routing and Planning
- Provide “User/Customer Design Guidelines” for BGA Routing on PCB.
- Provide Customer Reference Design for the BGA
- Provide Industry Standard Flotherm Model for the Package.

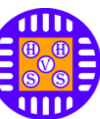


PACKAGE FEATURES SUMMARY

PACKAGE FEATURES	DESCRIPTION
Max Speed	Upto 56G (NRZ)
Package Design Tool	Allegro Package Designer (APD)
Package Simulation Tool	Cadence Sigrity / Ansys HFSS
Package Size	7x7 mm upto 75x75mm
Die Size	~2x2mm upto ~35x35mm
Minimum Bump Pitch	100um
Bump Type	BoP / BoT / Mixed
Package Nodes	40nm / 28nm / 14nm
Package Layer Count	0-2-0 upto 8-2-8
Max. Die Count	8 Dies within an mcm

INCOMING CUSTOMER COLLATERAL

- Project Timeline & Deliverables
- Preliminary Bump Map / Ball Map
- Stack-up & Signal Impedance Details
- Die/Package Shrink Factor (if available)
- Layout Guideline
- SI and PI Spec for high speed / Critical Interfaces.
- Constraints, if any
- Other specific requirements

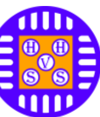


PACKAGE DESIGN FLOW

- Collect "Incoming Customer Collateral"
- Create Schematic & Import Netlist
- Set Constraints & Stackup
- Placement Complete
- Define Preliminary BGA BallMap
- Review Placement With Supplier
- High Speed Routing Complete
- Run SI Sims & Optimize Routing
- Route Sensitive / Analog Section
- Power Plane Routing Complete
- Review MCM with Supplier For DRC Violations
- Run PI Sims & Optimize Power Planes
- Finalize BGA BallMap
- Procure/Review TRA with Supplier
- 1-2 Rounds of Feedback with Supplier
- Run Checklists & Customer Approval
- Generate Flotherm Model
- Hand-Off Deliverables

QUALITY CONTROL

- Review Die vs BGA Schematic Connections – Functional Package First Time
- Review Final BGA Ball Map – Efficient Customer Board Design
- Run/Review the SI and PI report – Best Performance
- Review TRA and other feedback from vendor/Supplier – Package Qualification
- Review Flotherm Report – Thermal Issues at Customer End
- Multiple Reviews with Customers and Vendor/Supplier at various stages of Package Design
- Review MCM DESIGN Checklist – compilation of all design rules and customer collateral, final sign-off.



PACKAGE DELIVERABLES

DESIGN COLLATERAL

==================

- Final mcm
- Package Schematic
- Package Verilog Netlist (DFT)
- S-Parameters files with Simulation Report
  - SI Report with RL/IL/XTALK Plots
  - PI Report with per bump R & L Numbers
  - SPICE RLC file, if requested.

DESIGN REPORTS

============

- Package Design Checklist
- Package DRC Report
- Package Diff Pair NetLength Report
- Package Assembly Technical Risk Analysis(TRA) Report
- Package Flotherm Model (pdml file)

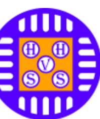
PCB MANUFACTURING SUMMARY

- Very Flexible Support Structure
  - Option #1 => PCB Fabrication Only.
  - Option #2 => PCB Fabrication + Assembly (Consigned or Turnkey)
  - Option#3 => PCB Fabrication + Assembly + BringUp/Test
- Partner with top domestic and offshore PCB manufacturer
- Quick Turn Prototype or High Volume Production PCBs
- Can Bringup and Test the board as per customer requirement / guidelines.
- Can ship the finished goods directly to customer inventory/warehouse.

SIMULATION TOOLS

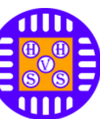
- SIGNAL INTEGRITY SIMULATION TOOL
  - Ansys HFSS 3D Layout
  - Cadence Sigrity 3DFEM
- POWER INTEGRITY SIMULATION TOOL
  - Ansys SIWave
  - Cadence Sigrity XtractIM

- THERMAL SIMULATION TOOL
  - Flotherm (PDML FILE)



PRE-LAYOUT ANALYSIS

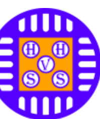
- Perform detailed SI analysis of high-speed parallel buses and serial links
- Perform die-to-die analysis pre-layout, post-layout, or anywhere in between
- Verify interfaces will be compliant with interface performance standards
- Concurrently evaluate SI effects such as losses, reflections, crosstalk, and simultaneous switching output (SSO)
- Observe the impact of non-ideal power delivery system effects on system behavior
- Reduce costs and time by identifying potential problems early
- Quantify the BER and performance of complex SerDes channels
- Advanced parallel-bus (DDR) and serial-link (SerDes) analysis



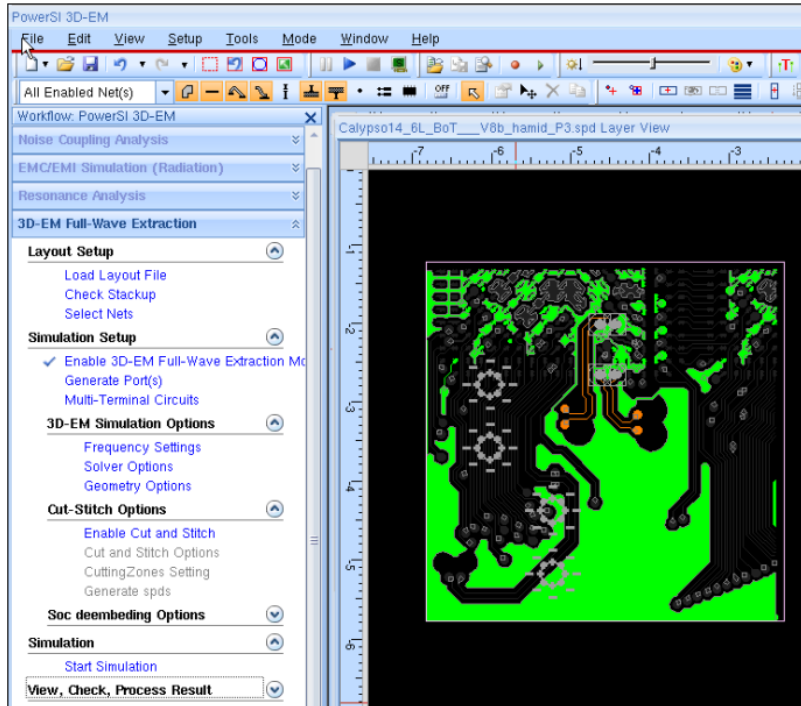
SIMULATION SUMMARY

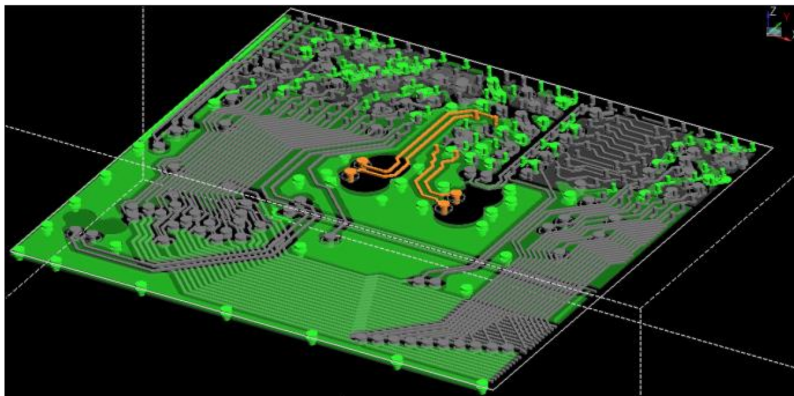
- SI / PI Simulation for PCB & Packages :
  - Will provide detailed PowerPoint Report
  - SI Section of the Report will include Stackup Data / Diff Pair Geometry Calculation Table / S-parameter Files & Plots.
  - PI Section of the Report will include “Electrical Performance Assessment” Report which will show RLC parameters for each Silicon Bump.

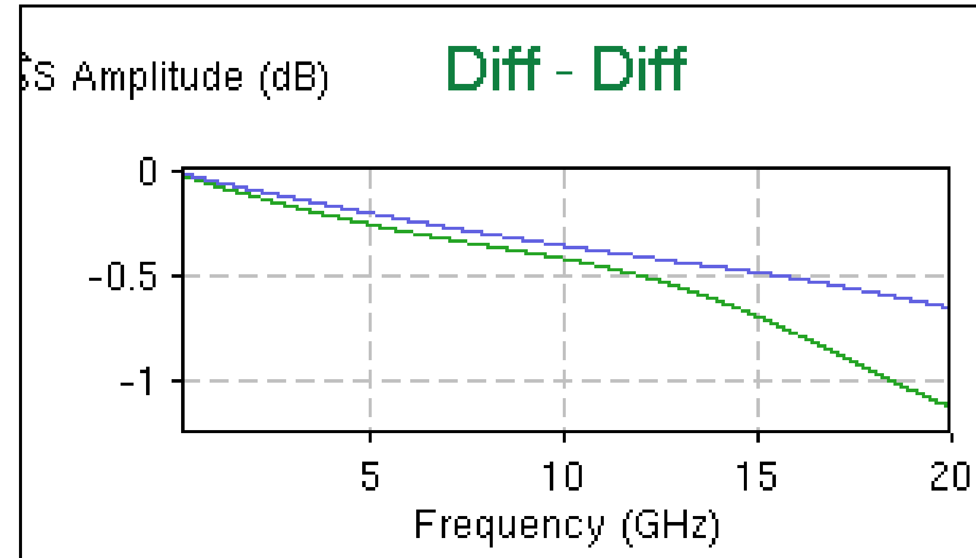
- Thermal Simulation (Flotherm Model) for PCB & Packages :
  - Will provide Industry Standard Flotherm Model in .pdml format showing standard thermal parameters like Theta Jc.
  - Will provide a corresponding pdf report

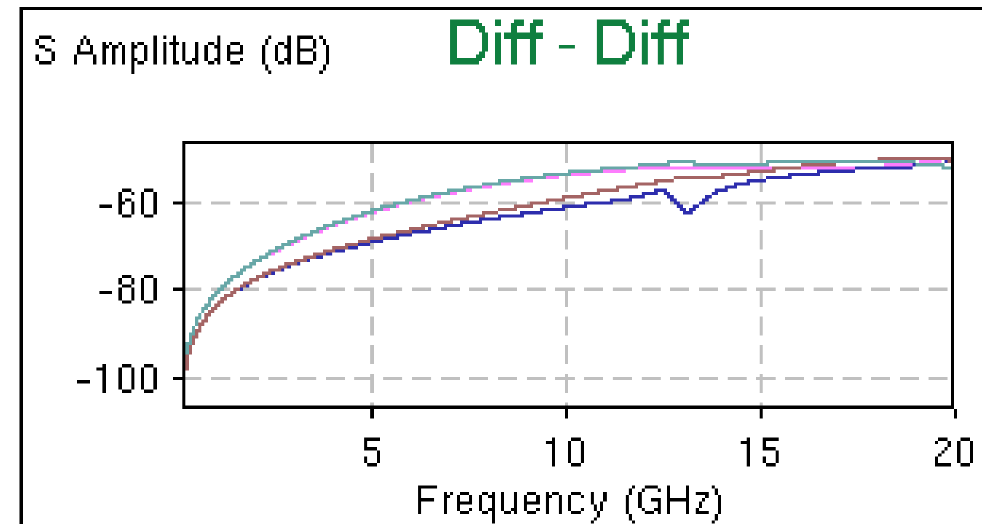


SIGNAL INTEGRITY : IL & XTALK









SIGNAL INTEGRITY : RETURN LOSS

PowerSI 3D-EM

File View Operation Window Help

Workflow: PowerSI 3D-EM

- Noise Coupling Analysis
- EMC/EMI Simulation (Radiation)
- Resonance Analysis
- 3D-EM Full-Wave Extraction

Layout Setup
- Load Layout File
- Check Stackup
- Select Nets

Simulation Setup
- Enable 3D-EM Full-Wave Extraction Mc
- Generate Port(s)
- Multi-Terminal Circuits

3D-EM Simulation Options
- Frequency Settings
- Solver Options
- Geometry Options

Cut-Stitch Options
- Enable Cut and Stitch
- Cut and Stitch Options
- CuttingZones Setting
- Generate spds

Soc deembeding Options

Simulation
- Start Simulation

View, Check, Process Result

Generate Model

S Amplitude (dB)

Differential Channel V | S | Amplitude | Impedance Curve Mask

Network Parameters
- Sdiff1 (Imp:50.000000) - (/u/hcostas
  - Mode Definitions
  - Diff - Diff: SDD[1,3], SDD[1,4], SDD[2,4], SDD[3,2]
  - Diff - Comm: SDC[1,3], SDC[1,4], SDC[2,4], SDC[3,2]
  - Comm - Diff: SCD[1,3], SCD[1,4], SCD[2,4], SCD[3,2]
  - Comm - Comm: SCC[1,3], SCC[1,4], SCC[2,4], SCC[3,2]

Isolated Curves

S Amplitude (dB) Diff - Diff
-50, -60, -70, -80, -90, -100
5, 10, 15, 20
Frequency (GHz)
SDD[1,3] SDD[1,4

S Amplitude (dB) Diff - Comm
-40, -50, -60, -70, -80, -90, -100
10, 20
Frequency (GHz)
SDC[1,3] SDC[1,

S Amplitude (dB) Comm - Diff
-40, -50, -60, -70, -80, -90
5, 10, 15, 20
Frequency (GHz)
SCD[1,3] SCD[1,4

S Amplitude (dB) Comm - Comm
-30, -40, -50, -60
10, 20
Frequency (GHz)
SCC[1,3] SCC[1,

POWER INTEGRITY : SELF INDUCTANCE/RESISTANCE

XtractIM - PI_Example.ximx - PI_Example.spd

Workspace Edit View Mode Setup Tools Window Help

Extractor Result

All Enabled Net(s)

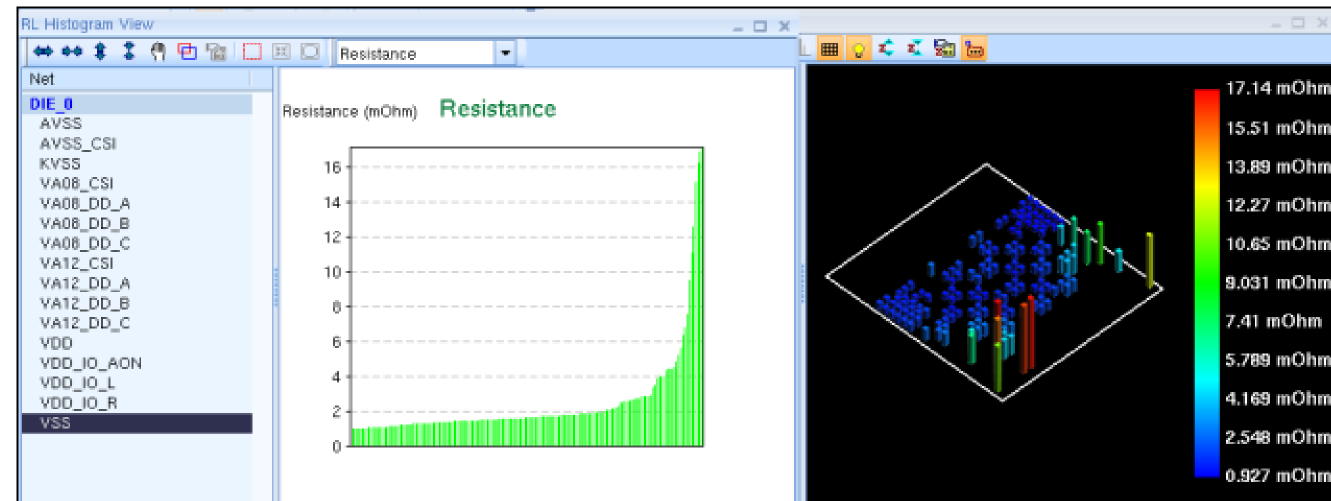
Workflow: XtractIM

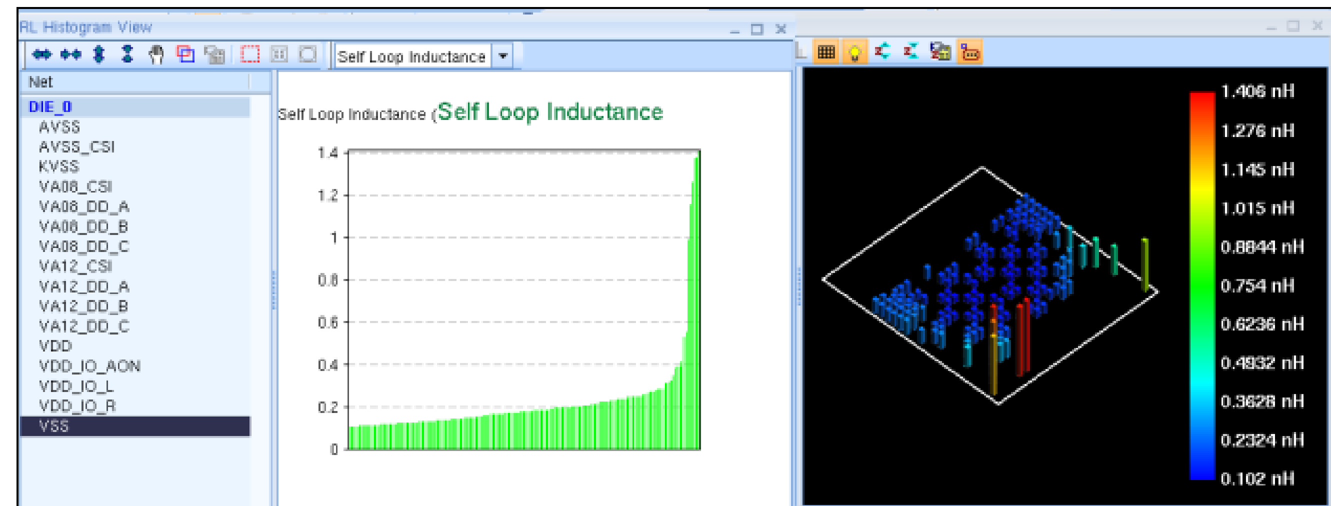
Model Extraction

Electrical Performance Assessment

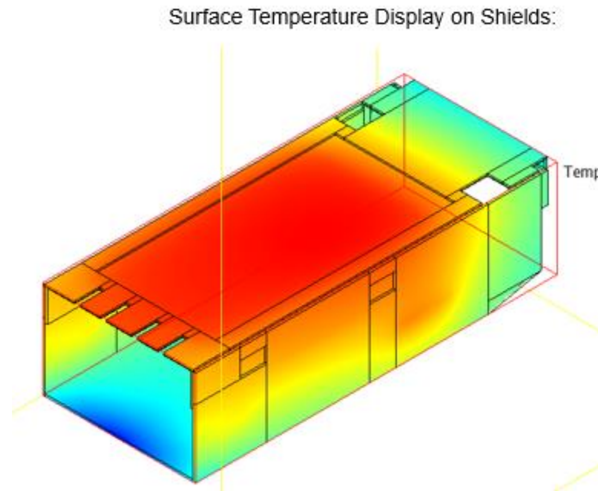
- Manage Workspace
  - Load Workspace
  - Load a New/Different Layout
- Simulation Mode
  - Enable Electrical Performance Assessment
- Package Setup
  - Package Type: Flip-Chip
  - Components
  - Stackup
  - Bumps
  - Solder Ball
  - Nets
- Simulation Setup
  - Setup for Power-Ground Analysis
  - Setup for Signal Analysis
  - Setup for Current Checking
- View/Export Results
  - Power-Ground Analysis
    - Per Net-Pair Properties
      - Inductance and Capacitance
    - Per Pin Properties
      - R&L Histogram
      - R&L by Layer
      - R&L Distributions
      - R&L Per Pin
      - R&L 2D View
  - Save Result
  - Load Result
  - Report

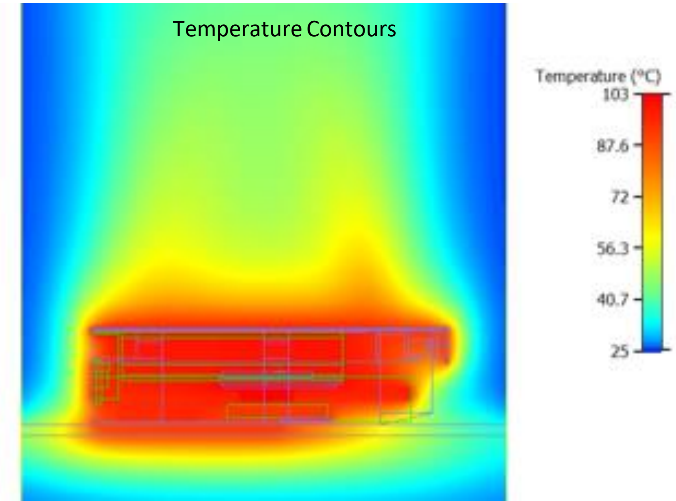
PI_Example.spd Layer View



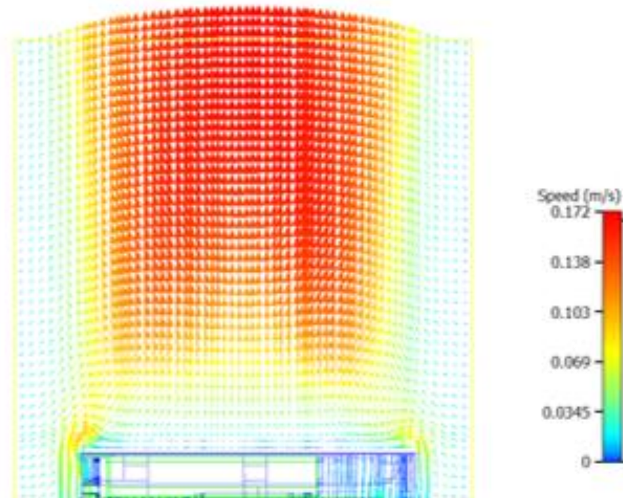


PCB FLOTHERM MODEL

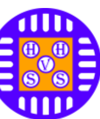




An overall velocity vector plot:



Will work with 3rd party vendor to get the Flotherm Model for the PCB with/without Enclosure



PACKAGE FLOTHERM MODEL

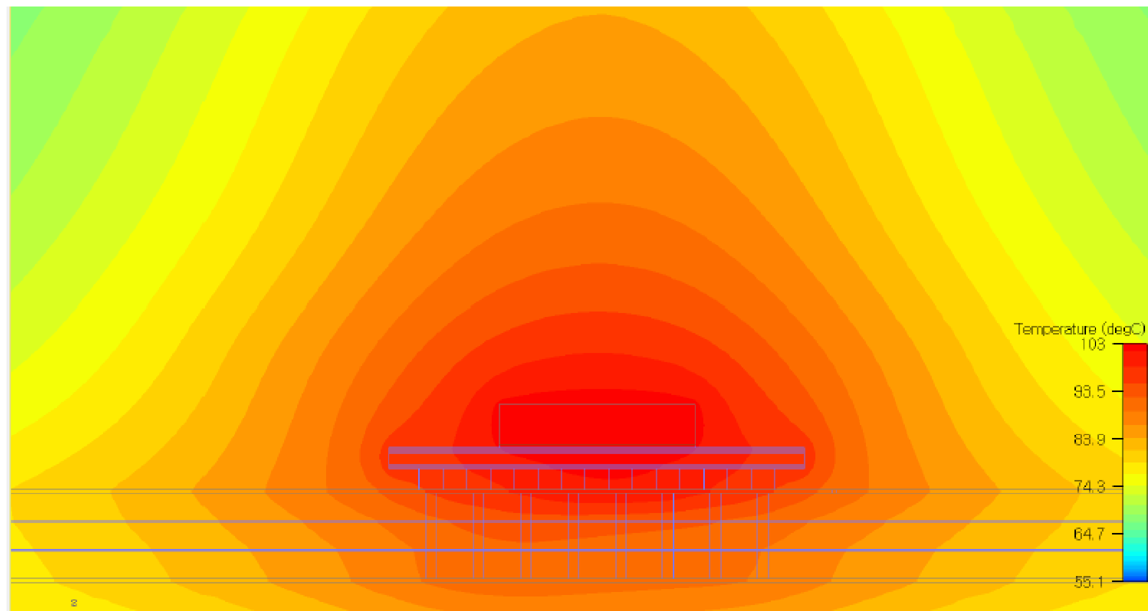
5. Software Information

Software	Flomeric FloTHERM V11.3
Modeling Technique	Computational Fluid Dynamics

6. Results

Ambient Temperature (°C)	55 °C					
Power	2.5 W					
Air flow(m/s)	T_J (°C)	T_T (°C)	T_B (°C)	Θ_{JA} (°C/W)	Θ_{JC} (°C/W)	Θ_{JB} (°C/W)
Detailed	103.11	102.88	91.12	19.24	0.22	5.01
Simplified	103.14	102.90	91.43	19.26	0.22	4.91

7. Plot



Will work with 3rd party vendor to get the Flotherm Model for the Package with/without Heat Spreader

THANK YOU

HVSTECH LLC

2622 Meadow Glen Dr,
San Ramon, CA 94583
USA
Email : info@hvstechllc.com
Phone : 1-408-406-1118